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Design of a current Mode Sample and Hold Circuit at sampling rate of 150 MS/s

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Abstract:
A current mode sample and hold circuit is presented in this paper at 180nm technology. The major concerns of VLSI are area, power, delay and speed. Hence, we have used a MOSFET in triode region in the proposed architecture for voltage to current conversion instead of a resistor being used in previously proposed circuit. The proposed circuit achieves high sampling frequency and with more accuracy than the previous one. The performance of the proposed circuit is depicted in the form of simulation results.
Keywords: Sample and Hold, Current Mode Circuits, CMOS

I. Introduction

Digital signal processing finds its great importance in several applications such as video and audio processing systems, image processing systems and instrumentation etc. The analog to digital converter is an interface between the digital signals and analog signals. Sometimes the signal degrades due to its conversion from the analog to digital or vice-versa. So, to avoid this degradation from ADC the sample and hold circuits are required at the input stage. The sample and hold circuits have been continuously modified in the past. Earlier, the switch was implemented by a single MOS transistor but the resistance of the switch varied according to the switch voltage. In order to remove this effect bootstrapped switched were employed as these switches provided constant gate-source voltage for the MOS switch to prevent variations in resistance.
In this paper we have presented a CMOS current mode sample and hold circuit for the realization of higher speed, higher accuracy and reduction in size of the circuit to decrease the area as it is most important factor in terms of VLSI. The proposed circuit is being modified with the MOSFET replacing the resistance. The remaining sections of the paper explain the current mode circuits, the design of folded cascode op-amp used and the last section discusses the final design and conclusion of results.

A Basic Sample and Hold Circuit

A conventional representation of current mode sample and hold circuit is shown in fig.1. If the charge injected by S1 generates a small deviation in the gate-source voltage (ΔVGS), the output current will have an error equal to $\Delta VGS.g_m$ where *gm* is the transconductance of M1. Since *gm* itself depends on input/output current, even if the charge injected by S1 is somehow made signal independent, its effect will still appear as a signal dependent current at the output. The solution is to make the V/I relation of the circuit as linear as possible (i.e. making g_m constant).

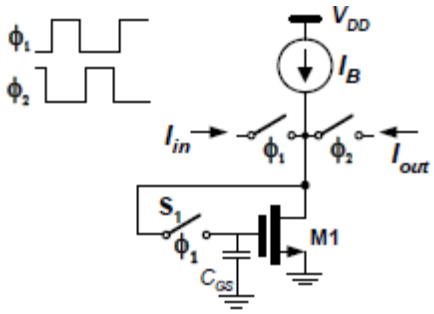

Fig.1. Basic Sample and Hold Circuit

Amplifier

The proposed sample and hold circuit uses a two stage amplifier. With a folded cascode differential input amplifier as first stage and a common source amplifier at the output stage the op-amp provides a total gain of 88.52 dB for a bit accuracy of 13 bits and unity gain frequency of 1.12 GHz for higher sampling rate. Gain error is given as:

Gain error = $x = \frac{1}{1+\text{Loop gain}}$ <= 0.5 LSB

The schematic of the differential cascode amplifier is shown in fig.2 a high swing cascade current mirror has been used as a load in the first stage.

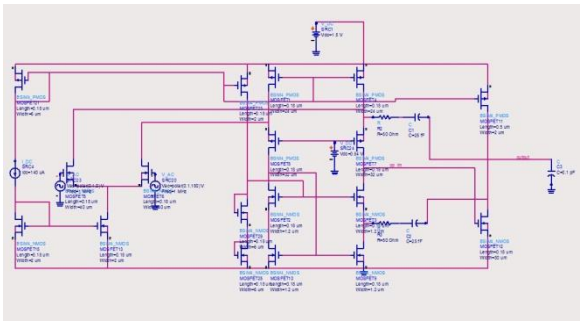

Fig.2 The two stage amplifier

The two stage operational amplifier has differential input stage while it has a single ended output. The first stage of the amplifier is differential cascoded which produces a single ended output using the current mirror load. The second stage of the amplifier is common source amplifier with PMOS load to attain high output swing.
In first stage the higher gain is achieved due to differential cascode input stage while in second stage the higher output swing is achieved whereas the gain of output stage is not considerable and it is low.

Proposed Architecture of Sample and Hold Circuit

The proposed architecture of the sample and hold circuit is shown in fig.3.

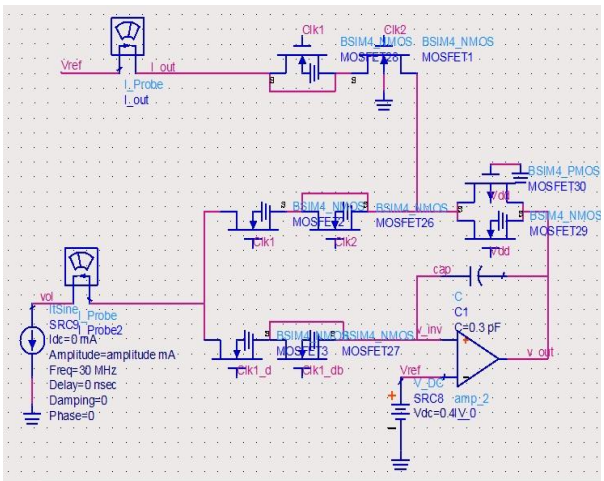

Fig.3 Proposed Sample and Hold Circuit Schematic

During sampling phase (φ1), the capacitor is charged up to $VC=RI_{in}$. In the following hold phase, *VC* is kept unchanged, and switch S3 connects *R (The parallel connected MOSFETs)* to the next stage. The on resistance of a MOSFET when (VDS << 2(VGS-VTH)) is given as

$$Ron = \frac{1}{\mu Cox\,(W/L)(Vgs - Vth)}$$

Assuming the input of the next stage is held at V_{REF}, the output current in the hold mode will be the same as input current at the end of the sampling mode, i.e.

$$I_{out}[n] = \frac{Vref - Vo[n]}{R + Ron} = I_{in}[n-1]$$

Where R_{on} is the on-resistance of the matched switches S1 and S3 and V_o is the output voltage of the amplifier. As all the switches within the circuit are connected to a constant voltage, any variation in the on resistance of the switches related to input voltage level is removed. This, in turn, reduces the overall distortion of the circuit. Furthermore, the above property makes it possible to have a large and constant gate-to-source voltage for each of the switches. Therefore neither complimentary switches nor clock boosting techniques are needed, provided that the reference voltage (VR_{EF}) is properly selected.

II. Simulation Results

The input and output waveforms of the proposed architecture is shown in the fig.4. The sampling frequency is 150 MS/s and the frequency of input current signal taken is 30 MHz with amplitude of 0.5mA.

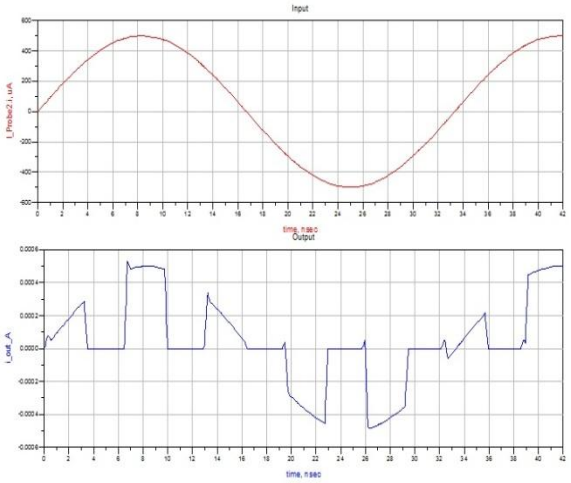

Fig.4. Input and Output Waveforms of proposed architecture

The following table (table.1) shows the specifications of the amplifier designed for the presented current mode sample and hold circuit.

Unity gain freq. (f_u)	1.12GHz
Phase margin	55.2^o
Power consumption	1.55mW
Output swing	1.2V @1.5V
C_L	0.1pF
DC gain	88.52dB

Table.1. Amplifier specifications

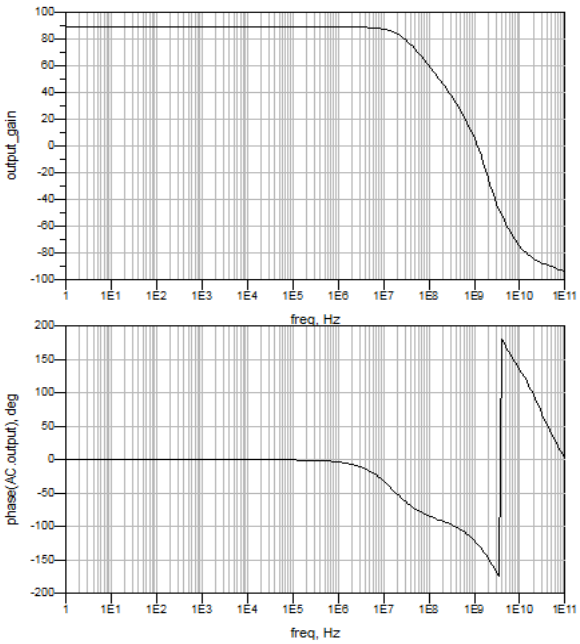

Fig.5 Gain and Phase Margin Plots of the amplifier

The gain of the proposed amplifier has higher gain than the conventional as it approaches to 88.52dB with a phase margin of 55.2 degrees. The switches used in the design have dummy switches with complementary clock input to reduce charge injection. The width (W) of the dummy transistor has been kept two times (2W) of the NMOS switch used.

Parameter	Prev. design	Proposed
Sampling freq. (F_s)	150MS/s	150MS/s
Power	3.7mW	3.42mW
V_{dd}	1.5V	1.5V
Bit resolution	12 bits	13 bits
Technology node	180nm	180nm

Table.1. Comparison with previous design

III. Conclusion

We have designed a two stage cascade amplifier and a sample and hold circuit with higher gain and less area in comparison to the previously proposed sample and hold circuit [3] at 180nm technology. The comparison shows that the design consumes less power than previous design and has more resolution.

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